Via Arrays for Grounding in Multilayer Packaging – Frequency Limits and Design Rules

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Abstract — **Many packaging concepts use via arrays for grounding and to eliminate parasitic modes. Such arrays represent periodic structures and change their behavior beyond a certain frequency. Proper design of via geometry and pitch is necessary. For this purpose, electromagnetic simulation data and an equivalent circuit model are presented.**

I. Introduction

Multilayer structures are widely used in state-of-the-art mm-wave packaging. They allow high integration density as well as cost efficient fabrication. Fig. 1 presents an example: a GaAs MMIC is mounted on top of an LTCC carrier substrate. Instead of inserting a solid metal pedestal into the LTCC substrate below the chip as electrical ground and heatsink, this function is realized by an array of grounding vias.

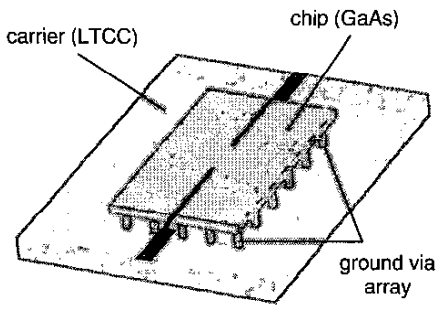

Fig. 1. Multilayer structure with microstrip environment. The backside of the LTCC carrier is connected to the GaAs chip ground plane using a 5×6 via array.

Such via arrays, however, exhibit filter characteristics due to their periodic nature and can be considered as photonic-bandgap structures [1]. Beyond a certain frequency, passbands are observed, within which the desired grounding mechanism disappears and parasitic coupling occur. Via pitch and diameter have to be chosen properly, so that the critical frequency bands are moved to a range beyond the frequency of operation. Such effects are known particularly for packaging structures [2], e.g., ceramics or LTCC boards, where minimum via pitch and diameter reach the wavelength's order of magnitude already for the mm-wave frequency bands around 40 GHz. Similar effects are observed on-chip for frequencies beyond 100 GHz, e.g., when applying vias for grounding in coplanar structures [3]. Simple design rules using a half-wavelength pitch are found to yield approximations too inaccurate for most practical cases.

Hence, an understanding of the physical effects and more precise design rules are required for via placement in package development. This is the purpose of this paper. Based on three-dimensional electromagnetic (em) simulations we develop an equivalent-circuit description, which provides an easy-to-handle tool for design.

Our investigations show that the via array can be treated as a sequence of lateral via fences. An equivalent-circuit description is derived for a single fence. Its element values for different substrate thicknesses, via geometries, and pitch values are given covering the common ceramics and LTCC structures. Connecting these circuits in series results in a description for the entire via array.

Moreover, parasitic wave propagation may occur along the borders of the patch if the distance from the patch edge to the outer vias is too large. Even this effect is addressed separately in Sec. III.

II. Modeling Approach

In order to study the behavior of the via array, first laterally infinite arrays are investigated. The problem thereby simplifies to a parallel-plate line between magnetic walls, which is shortened by a row of vias, as shown in Fig. 2 for the case of 2 vias. The structure is excited with the parallel-plate (PPL) mode. The em simulations were carried out using the CST Microwave Studio software, which is based on the FDTD method.

The simulations showed that these structures can be modeled by a lumped equivalent circuit representing the single via fence, and connecting them in series via transmission lines. While the properties of these lines are readily given by propagation constant and impedance of the parallel-plate line, the parameters of the equivalent circuit for via fence are yet to be determined. Once this is done, however, the band pass behavior of structures consisting of

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an arbitrary number of via fences can be analyzed by common circuit simulators.

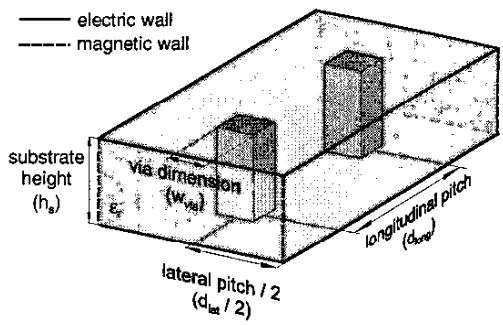

Fig. 2. Reference structure for via array modeling. Parameters are the longitudinal and lateral via pitch, substrate thickness h_s, its relative permittivity ε_r, and the via dimension.

The canonical equivalent circuit describing a single via fence is shown in Fig. 3. It consists of two serial inductances L_l and an LC resonant branch. The serial elements L_l represent the longitudinal current flow and a part of the via inductance. L is related to the mutual inductive coupling through the via and C describes the first resonance caused by the lateral via pitch.

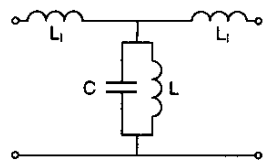

Fig. 3. Equivalent circuit model for a single via fence.

The parameters are extracted from em simulation data of a single-via structure according to Fig. 2 after deembedding of the parallel-plate line lengths between the ports and the via.

The interconnecting line segments between the via fences are given by the longitudinal via pitch and the parallel-plate line impedance

$$Z_l = \sqrt{\frac{\mu_0}{\varepsilon_0 \varepsilon_r}} \cdot \frac{h_s}{d_{lat}}$$

with h_s denoting the substrate thickness and d_{lat} the lateral via pitch.

Fig. 4 presents the results for via arrays with an increasing number of fences in longitudinal direction. A parameter set typical for LTCC substrates is chosen (see caption of Fig. 4). At low frequencies, the magnitude of input reflection is unity, i.e., the via array acts as a short and a small inductance as desired. Increasing the frequency, however, resonances are observed, the number of which increases with the number of via fences, eventually yielding a continuous passband. This frequency range is critical for most applications since the grounding function of the array is not effective any more. Therefore, the useful frequency range extends from DC to the onset of the first passband. It can be adjusted by choosing the via array parameters properly.

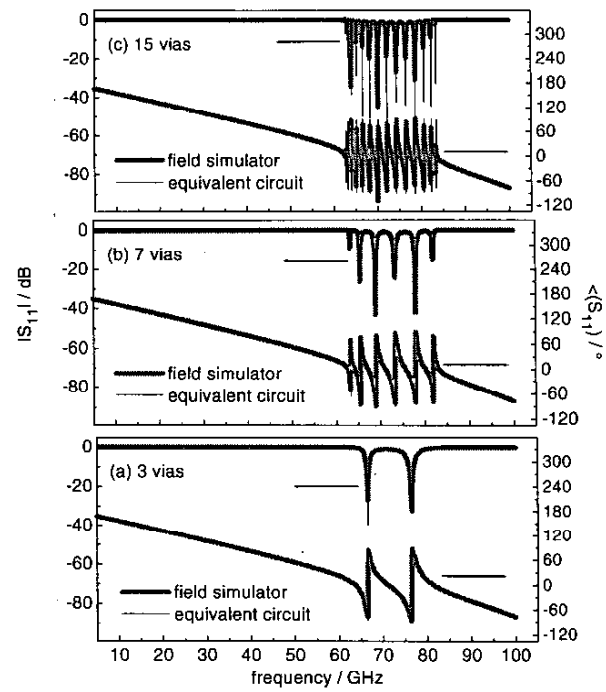

Fig. 4. Input reflection (magnitude and phase) against frequency for a via array according to Fig. 2 with 3, 7, and 15 via fences in longitudinal direction: equivalent-circuit description (Fig. 2) and FDTD data; the dimensions and material parameters are: longitudinal and lateral via pitch $d_{long}=d_{lat}=700\mu m$, substrate thickness $h_s=270\mu m$, via size $140\times140\ \mu m^2$, substrate permittivity $\varepsilon_r=7.8$. The corresponding equivalent-circuit parameters for the single via fence are $L_l=21pH$, L=22pH, C=75fF, the characteristic impedance of the PPL line connecting the via fences is 52Ω.

First, it is important to note that the lower corner frequency of the first passband is significantly lower than the cut-off frequency derived by a simple half-wavelength resonance. For the given structure, this criterion yields a value of 77 GHz for 700μm via pitch. As can be seen, however, the usable frequency range according to Fig. 4 ends already slightly above 60 GHz. Additionally, this deviation varies with the dimensions of the structure, which is unacceptable for design and proves that a more accurate model is required.

Comparing the em simulation results with our equivalent-circuit description one finds excellent agreement. This

verifies accuracy of the network approach based on the single-via circuit of Fig. 3. In the following, the dependencies of the equivalent circuit elements on the array parameters are studied (the substrate and via data refer to an LTCC board).

A. Variation of Substrate Permittivity and Thickness

Substrate permittivity ε_r affects only the capacitance C, which increases linearly with ε_r, the inductances L and L_l remain constant. This is in accordance with physical arguments.

Changing substrate thickness h_s, on the other hand, causes a linear scaling of both inductances while the capacitance varies with $1/h_s$. As a consequence, the S parameters and thus the passband corner frequency do not change with substrate thickness.

B. Influence of Lateral Pitch and Via Size

The dependence on lateral pitch and via size is more involved than for substrate permittivity and thickness. First, the lateral pitch is studied. Fig. 5 presents the resulting element values for a via of 140µm edge length.

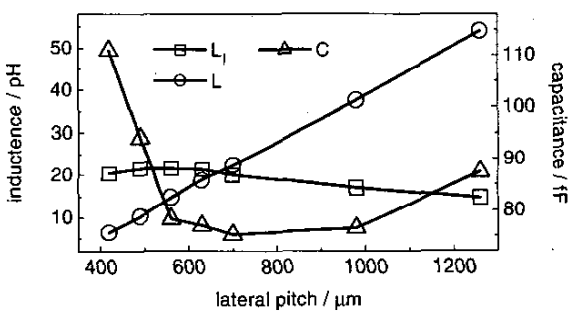

Fig. 5. Elements of circuit in Fig. 3 as a function of lateral via pitch; via dimension is 140×140µm², the substrate (ε_r=7.8) is 270µm thick. The lateral pitch is varied within in the range 420...1260µm, resulting in PPL impedances Z_l=87...29Ω.

The inductance L exhibits a linear behavior with increasing pitch, whereas the longitudinal inductance L_l is not changed strongly within the pitch range under investigation. The capacitance, on the other hand, shows a distinctive nonlinear behavior, though the range is limited (75..110 fF).

Fig. 6 provides the corresponding data when varying the via cross-section. While the longitudinal inductance L_l is not strongly affected by an increasing via size, the inductance L decreases significantly, as does mutual coupling, and simultaneously the capacitance C increases.

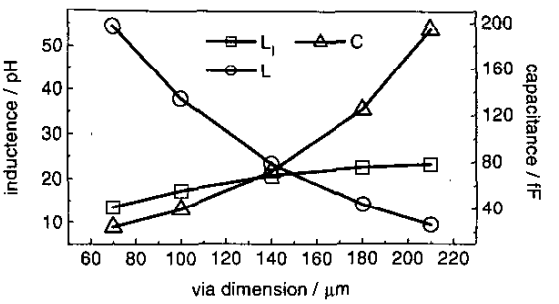

Fig. 6. Elements of circuit in Fig. 3 as a function of the via dimension. The edge length of the quadratic via is increased from 70µm up to 210µm. Lateral via pitch is 700µm, substrate permittivity is 7.8, resulting line impedance is 52Ω.

C. Resulting Design Rules for Via Arrays

While the previous sections treat the data for the single-via equivalent circuit according to Fig. 3, this subsection summarizes the results for an array of five vias and presents them in terms of the useful frequency range (see Fig. 7). The frequency limit is defined as the frequency, where the first minimum value of the S_{11} passband is reached. This diagram illustrates, how strong the different parameters influence the resulting frequency limit and can be used directly as a chart for dimensioning via arrays in LTCC boards.

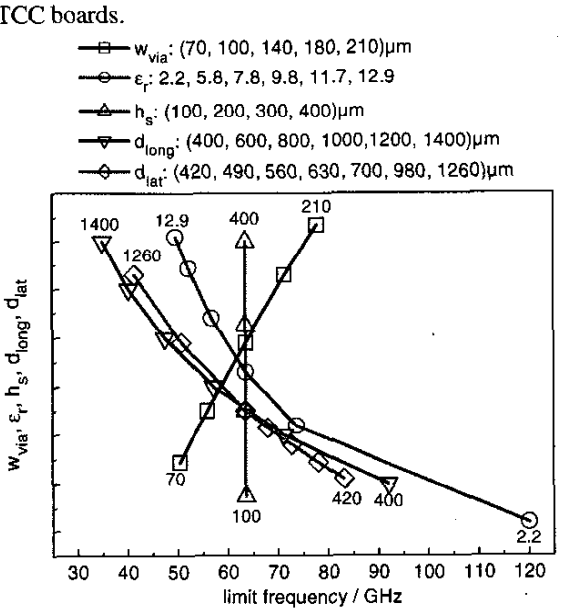

Fig. 7. Array parameters against frequency limit (first minimum of S_{11}) for a via array with 5 fences; parameter values as specified, the standard values are: Substrate of thickness h_s=270µm with ε_r=7.8, via size w_{via}=140µm, lateral via pitch d_{lat}=700µm, longitudinal pitch d_{long}=700µm.

III. FINITE VIA ARRAYS AND BORDER EFFECTS

The model for via arrays presented before assumes that the via array is of infinite extension in the lateral direction. To check validity of this simplification we simulated a structure comparable to Fig 1, with a 5×4 via array. The chip contains two opposite open stubs, which ideally should give very low transmission between the ports. The calculated results are shown in Fig. 8.

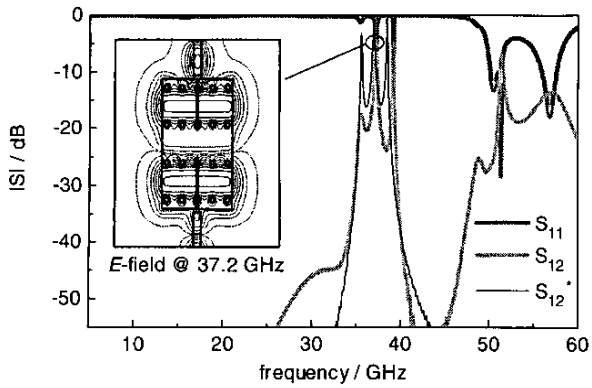

Fig. 8. S parameters for structure as in Fig. 1: GaAs chip (ε_r=12.9), 100µm thick, with two opposite microstrip stubs, chip size 3000 × 5000µm^2; LTCC carrier substrate (ε_r=7.8), 270µm thick; a 5×4 via-array is used (longitudinal via pitch 1430µm, lateral pitch 650µm, via dimensions 140×140µm^2). Plotted are FDTD data together with the results for S_{12}^* of our network model (thin line). The inset shows a field plot.

Up to 30 GHz, good isolation is obtained as desired. For higher frequencies, however, coupling effects inside the via array causes crosstalk between the two stubs (see the field plot in the inset of Fig. 8). Our model, which is based on the infinite lateral structure, predicts the frequency limit above 30 GHz with high accuracy (see thin line S_{12}^* in Fig. 8).

Generally, however, special attention has to be paid to the border of the patch, the unavoidable metallic overlap, which is determined by the distance between the outer via rows and the edge of the patch. In the structure of Fig. 8, this border is chosen to be 200µm. Choosing the border too large results in additional crosstalk due to wave propagation along the border area.

This effect can be illustrated easily choosing the above-described structure and increasing the border from 200 to 400µm (for a 5×5 via array). As can be seen from Fig. 9, now the first passband is observed at a much lower frequency than the modeled via-array frequency limit of 45GHz. For border widths smaller than 180µm, this specific crosstalk effect occurs at frequencies above the via-array limit and again we find good agreement between our frequency limit estimation and the em simulation.

Further work is in progress to allow accurate prediction of the frequency limits of this border effect.

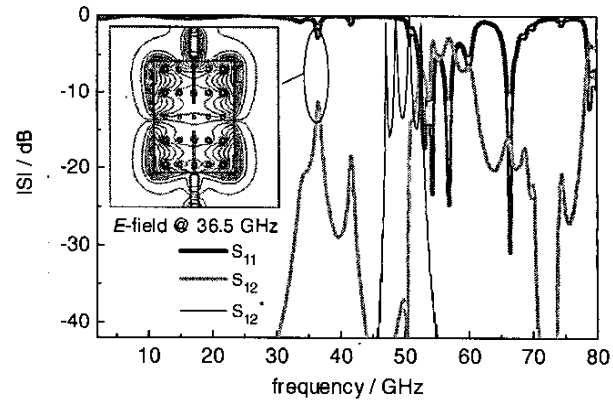

Fig. 9. Results of Fig. 8 for a structure with 400µm border width (broader chip and reduced longitudinal pitch): FDTD results and modeling (thin line); GaAs chip size 3600 × 5000µm^2, 5×5 via array with reduced longitudinal pitch of 1075 µm; all other data as in Fig. 8.

IV. CONCLUSIONS

Our results regarding the design of via arras used for grounding as chip pedestal may be summarized as follows:

Basic parameter is the via pitch, which determines the frequency limit above which the grounding effect vanishes. The simple half-wavelength rule for this frequency limit involves large uncertainties. The equivalent-circuit presented here allows accurate prediction and is scalable for any number of via fences.

The border of the patch (i.e., the distance between outer vias and patch edge) is a further critical parameter and has to be chosen as small as possible.

Further work is in progress to investigate the wave traveling effects at the patch borders in more detail and to develop a closed-form expression for the frequency limit of an array given its parameters.

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